FIG. 1

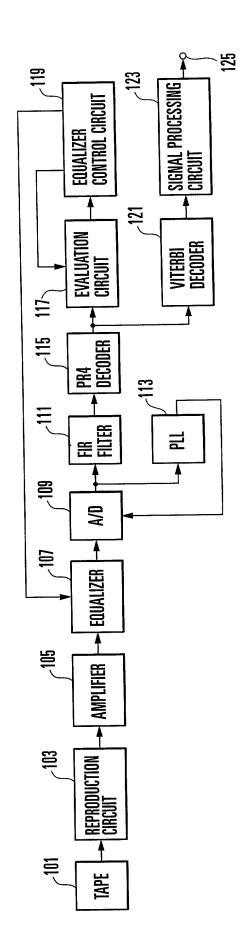
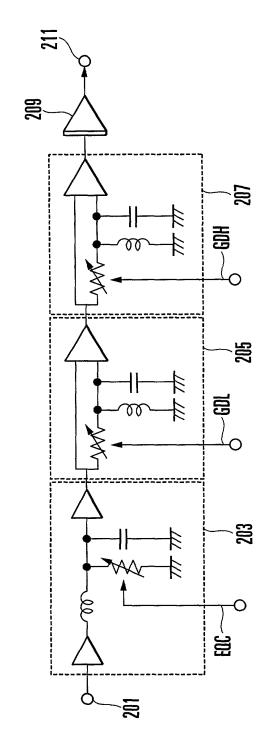
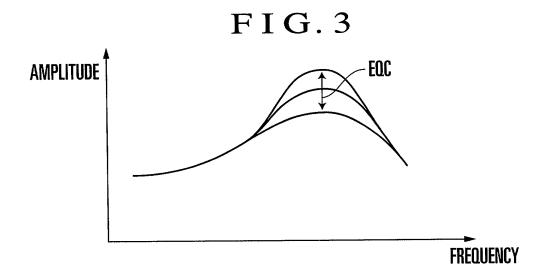
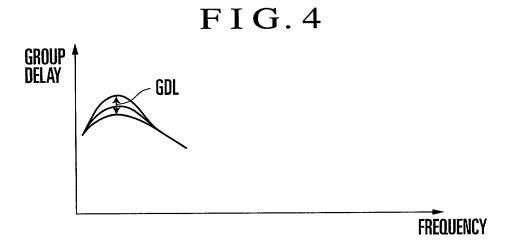


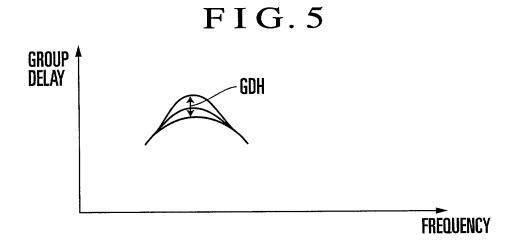
FIG. 2

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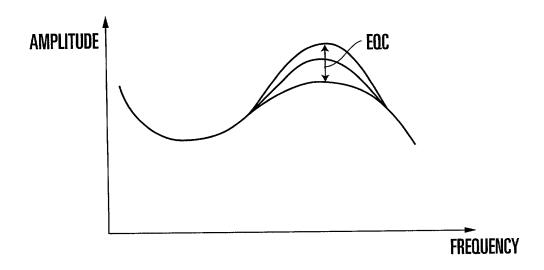








F I G. 6



F I G. 7

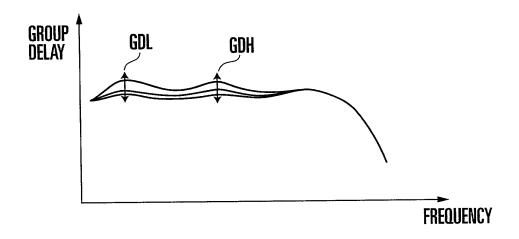


FIG. 8

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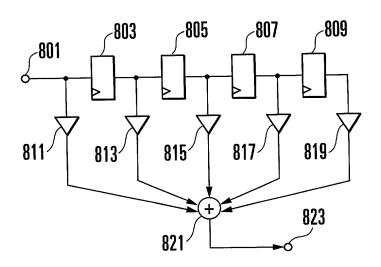
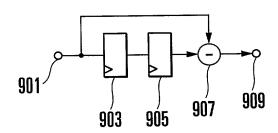
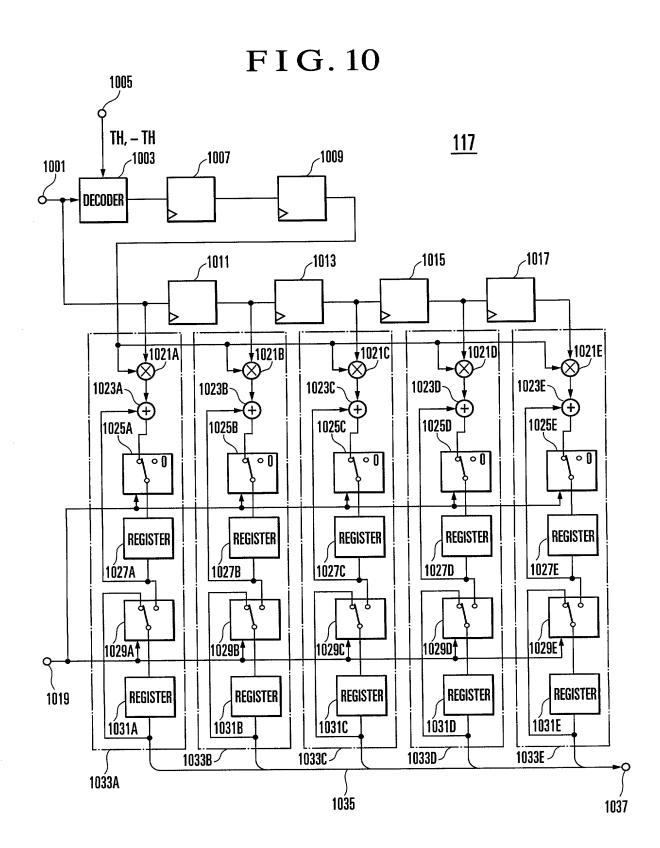
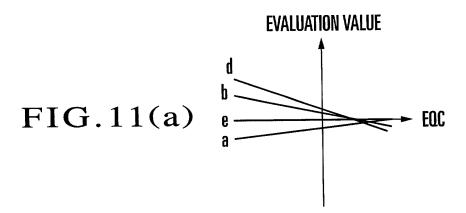


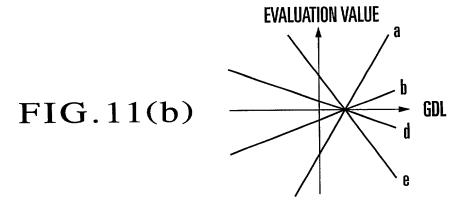
FIG.9

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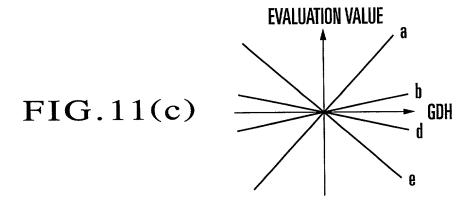
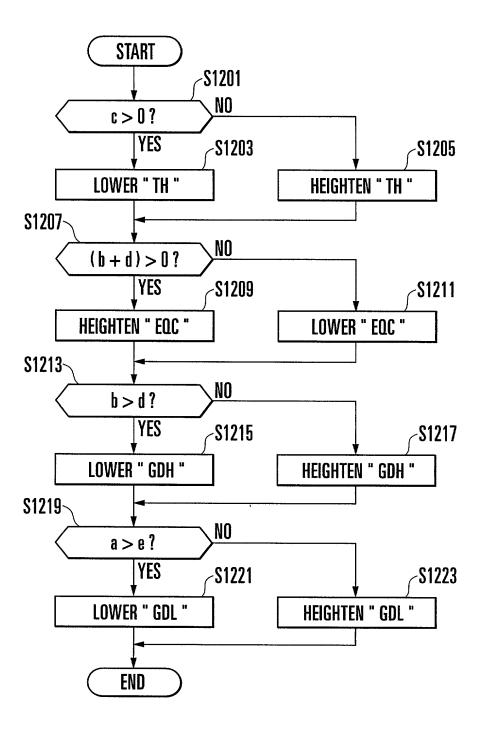


FIG. 12





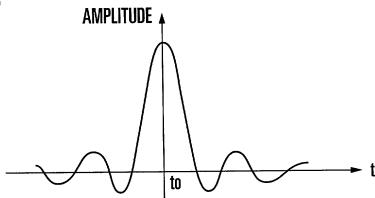


FIG.14(a)

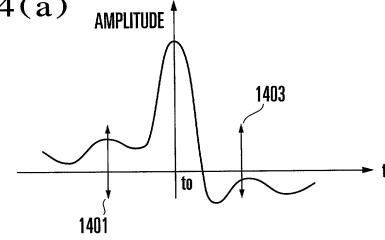


FIG.14(b)

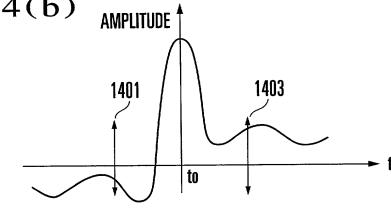


FIG.15(a)

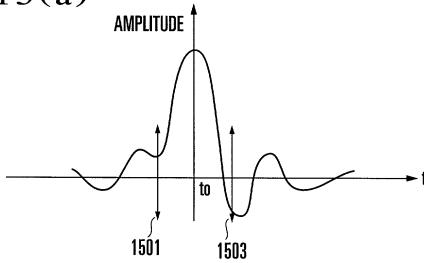


FIG.15(b)

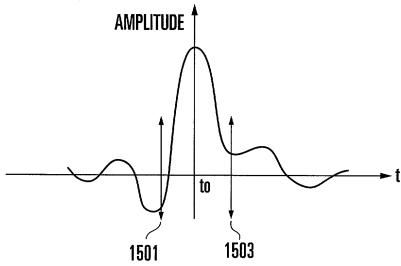
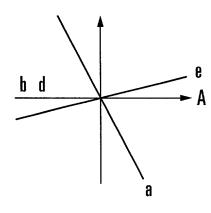


FIG.16(a)

FIG.16(b)



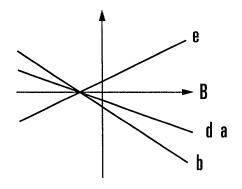
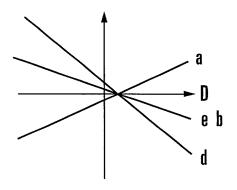
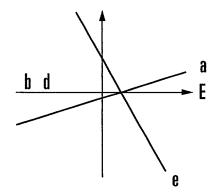


FIG.16(c)

FIG.16(d)





125 SIGNAL PROCESSING CIRCUIT 133 SYSTEM CONTROLLER OPERATION Switch 135 ERROR CORRECTION CIRCUIT EQUALIZER Control circuit 137 MEMORY 121 VITERBI DECODER PR4 DECODER 급 → EQUALIZER → A/D AMPLIFIER 103

FIG. 17

FIG. 18

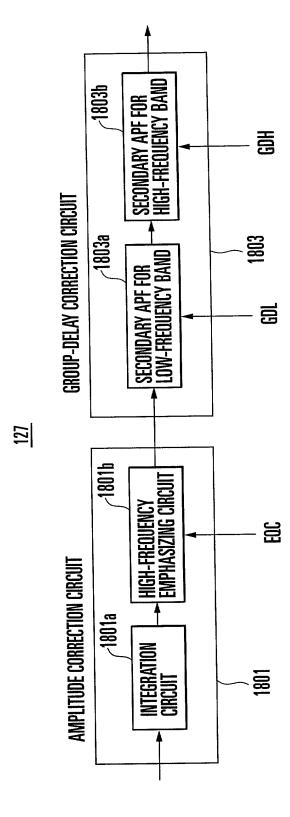


FIG.19 (a)

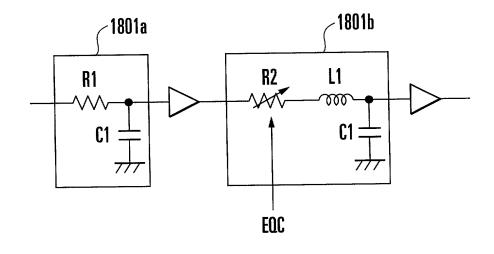


FIG.19(b)

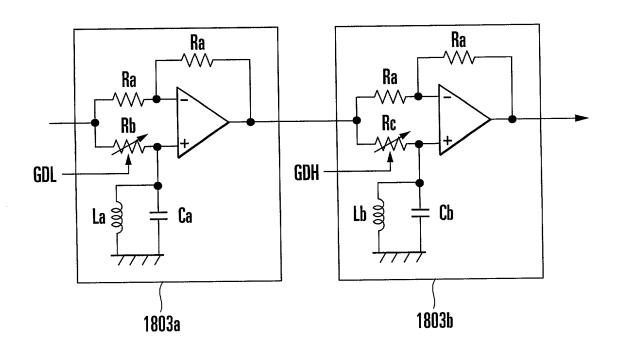
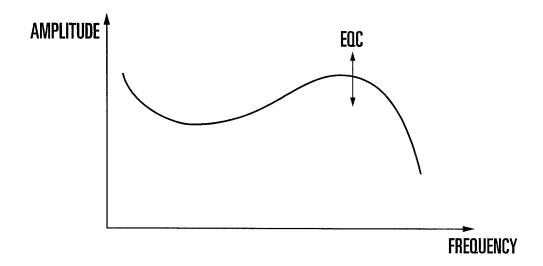
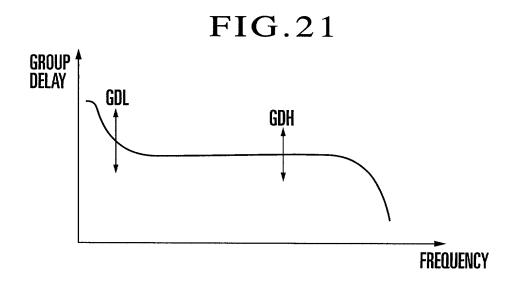
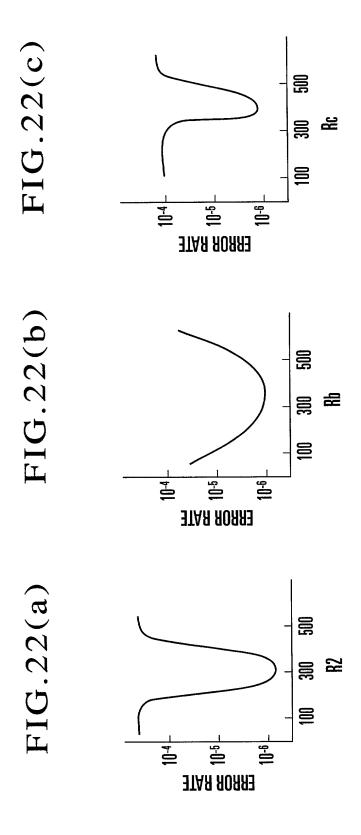


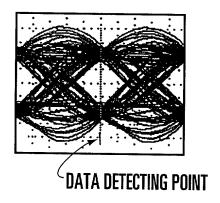
FIG.20







## FIG.23(a)



## FIG.23(b)

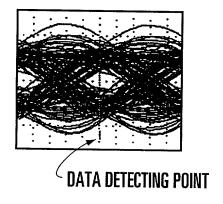


FIG. 24

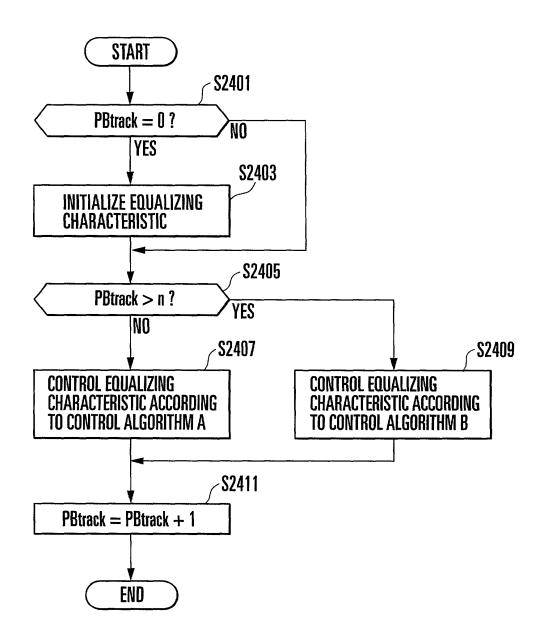


FIG. 25

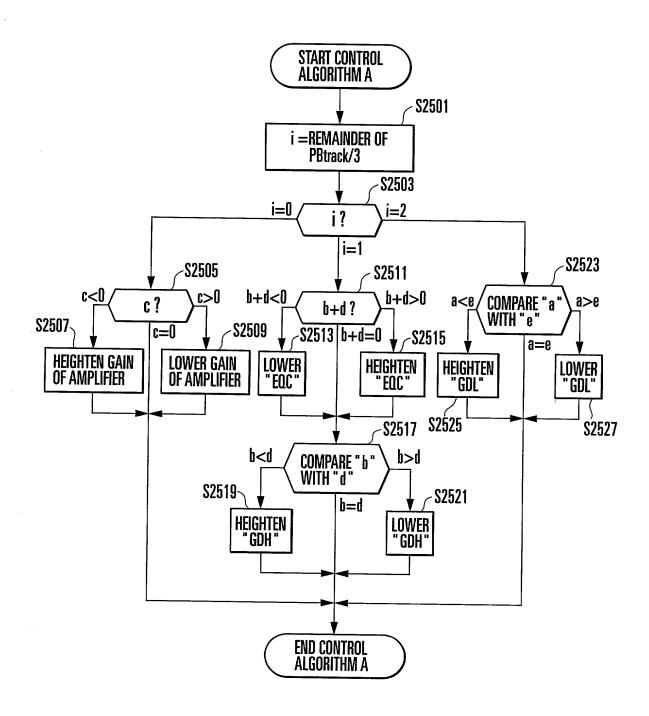


FIG. 26

